Abstract

Aspects of the present invention involve obtaining a sequence of logic transitions from an integrated circuit that are a function of one or more bits from the integrated circuit ("IC"). The logic transitions from the IC may be representative of one or more data values or bits. For each logic transition, a time is determined. From the time of each logic transition, the pattern of data values is derived. The pattern of data values may then be compared with an expected pattern of data values to test the IC.